What is claimed is:

1. A reset signal generating circuit for initiating an internal circuit of a semiconductor memory device, the circuit comprising:

an external voltage detector which detects a level of an external voltage and generates a first reset signal; and

a second reset signal generator which performs a logical sum of an external signal and the first reset signal, and outputs the result of the logical sum as a second reset signal,

wherein the second reset signal is used to reset a block related to a data path of the semiconductor memory device.

2. The circuit of claim 1, wherein the first reset signal is used to reset blocks other than the block related to the data path.

3. The circuit of claim 1, wherein the external signal is a clock enable signal.

4. The circuit of claim 3, wherein the second reset generator comprises:

an automatic pulse generator which generates a pulse signal which maintains a first logic level during a predetermined period in response to the clock enable signal; and

a logical sum gate which logically sums the pulse signal and the first reset signal, and outputs the result as the second reset signal.

5. The circuit of claim 3, wherein the block related to the data path further includes a data output driver for performing a driving operation for outputting the data through a pad, the data being output from a memory cell and then detected.

6. The circuit of claim 5, wherein the block related to the data path further includes a data input driver which performs a driving operation on the data which is externally input through the pad.

7. The circuit of claim 3, wherein the block related to the data path includes at least a part of a data output circuit in a path from an output node of an input/output sense amplifier which senses and amplifies the data output from a memory cell to an input/output pad.

8. A semiconductor memory device comprising;

a memory cell array;

a row decoder which selects and activates a word line of the memory cell array in response to a row address signal;

a column decoder which selects a column line of the memory cell array in response to a column address signal;

an input/output sense amplifier which senses and amplifies the data output from the memory cell array;

a data line driver for inputting the data in the memory cell array;

a data output unit which outputs through an input/ouput pad the data output from the input/output sense amplifier;

a data input unit which transmits the data input from input/output pad to the data line driver;

a control logic unit which generates a plurality of control signals in response to an address signal and a command signal; and

a reset signal generating circuit which generates a first reset signal and a second reset signal in response to an external voltage and an external signal,

wherein the data output unit is at least partially reset in response to the second reset signal.

9. The semiconductor memory device of claim 8, wherein the reset signal generating circuit comprises:

an external voltage detector which detects the level of the external voltage and generates the first reset signal; and

a second reset signal generator which performs a logical sum of a clock enable signal, which is externally input, and the first reset signal, and outputs the result of the logical sum as the second reset signal.

10. The semiconductor memory device of claim 9, wherein the second reset signal generator comprises:

an automatic pulse generator which generates a pulse signal which maintains a first logic level for a predetermined period in response to the clock enable signal; and

a logical sum gate which performs a logical sum of the pulse signal and the first reset signal, and outputs the second reset signal.

11. The semiconductor memory device of claim 9, wherein the second reset signal is also used to reset at least a part of the data input unit.

12. A method for resetting an internal circuit of a semiconductor memory device, the method comprising:

(a) detecting the level of an external voltage and generating a first reset signal;

(b) logically summing an external signal and the first reset signal and generating a second reset signal;

(c) resetting a block related to a data path in response to the second reset signal; and

(d) resetting blocks other than the block related to the data path in response to the first reset signal.

13. The method of claim 12, wherein the external signal is a clock enable signal.

14. The method of claim 13, wherein step (b) further comprises:

generating a pulse signal which maintains a first logic level for a period of time in response to the clock enable signal; and

performing a logical sum of the pulse signal and the first reset signal, and outputting the second reset signal.

15. The method of claim 13, wherein the block related to the data path further includes a data output driver for performing a driving operation for outputting the data through a pad, the data being output from a memory cell and then detected.

16. The method of claim 13, wherein the block related to the data path includes at least a part of the data output circuit in the path from an output node of an input/output sense amplifier which senses and amplifies data output from the memory cell to an input/output pad.